



Serial No.: 10/709,363
 Confirmation No.: 3362
 Applicant: Giovanni Gaviani et al.
 Atty. Ref.: 12693.0028.00US00

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently amended): A control system $[(19)]$ with multiprocessor architecture for an internal combustion powertrain $[(1)]$; the control system $[(19)]$ comprising a computing unit $[(20)]$ capable of executing both basic control functions of the powertrain $[(1)]$ and ancillary control functions not directly related to the control of the powertrain $[(1)]$; ~~the control system $[(19)]$ being characterized in that~~ the computing unit $[(20)]$ comprises
 - a main processor $[(21)]$ exclusively dedicated to executing basic functions for controlling the powertrain $[(1)]$;
 - at least one auxiliary processor $[(22)]$ dedicated to executing ancillary control functions, wherein the auxiliary processor can execute inter-processor interrupt operations in order to wait for the main processor to complete a particular computing algorithm, and the main processor does not execute inter-processor interrupt operations in order to wait for the auxiliary processor to complete a particular computing algorithm;
 - a number of memories $[(23, 24)]$;
 - a series of peripheral devices $[(25)]$;
 - at least one peripheral bus connection $[(26, 27)]$, to which the peripheral devices $[(25)]$ are connected $[,]$; and
 - a main bus connection $[(28)]$ through a cross-bar switch of the cross-bar bus type to allow the processors $[(21, 22)]$ to communicate with the memories $[(23, 24)]$ and with the peripheral bus connection $[(26, 27)]$ while avoiding the occurrence of conflicting communication operations.
2. (Currently amended): The control system $[(19)]$ of claim 1, ~~[[in which]]~~ wherein the computing unit $[(20)]$ comprises a first peripheral bus connection $[(26)]$, which is intended for connecting slow peripheral devices $[(25)]$, and a second peripheral bus connection $[(27)]$, which is intended for connecting high speed peripheral devices $[(25)]$.



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3. (Currently amended): The control system [(19)] of claim 1, [[in which]]wherein the memories [(23, 24)] comprise either RAM type memories [(23)] or ROM type memories [(24)] and can at least in part be protected, a first portion of the memories [(23, 24)] being reserved for the main processor [(21)], and a second portion of the memories [(23, 24)], different from the first portion, being reserved for the auxiliary processor [(22)].
4. (Currently amended): The control system [(19)] of claim 1, [[in which]]wherein the computing unit [(20)] comprises a single integrated circuit [(29)] that accommodates the processors [(21, 22)], the memories [(23, 24)], the peripheral bus connections [(26, 27)] and the main bus connection [(28)].
- 5-7. (Canceled)